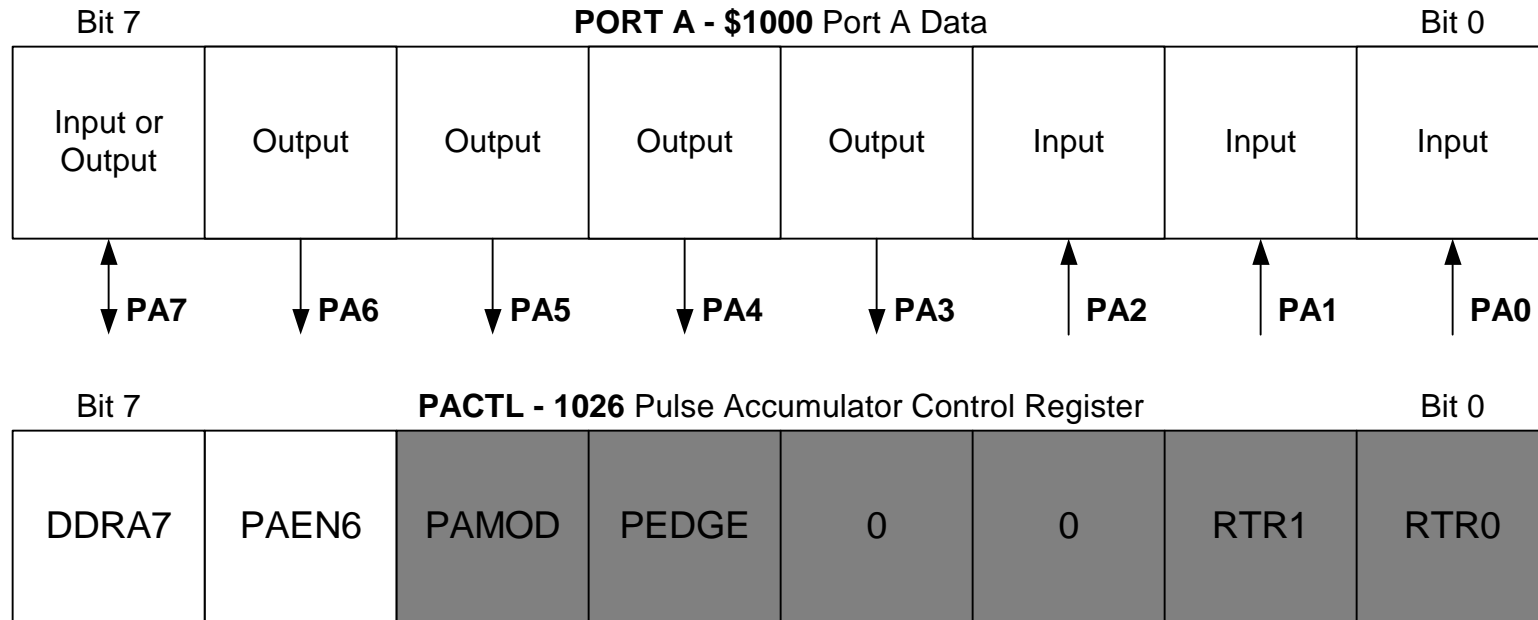


# Motorola 68HC11 PORT A

- Port A may be used as an 8-bit I/O port or it may be associated with timer and pulse accumulator functions. I/O functions can be interlaced with timer and pulse accumulator functions.
- PORT A DATA REGISTER: may be read or written into. If a bit is configured as an input it will not be affected by writing to it.



DDRA7 = Data Direction Register Bit A7. Input = 0, Output = 1.

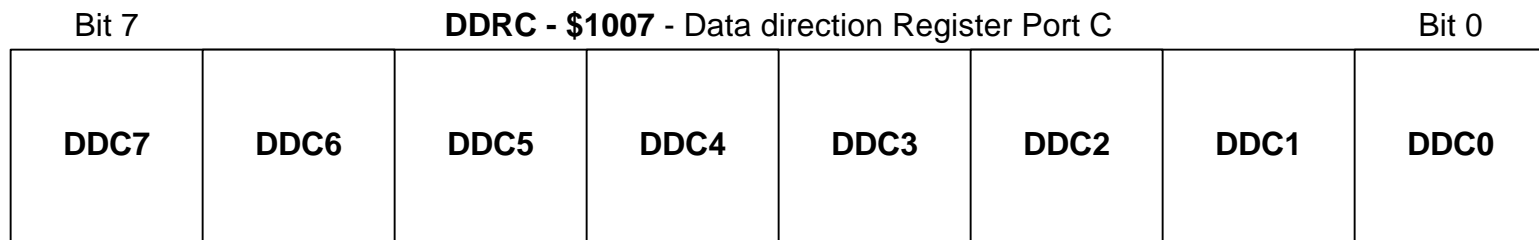
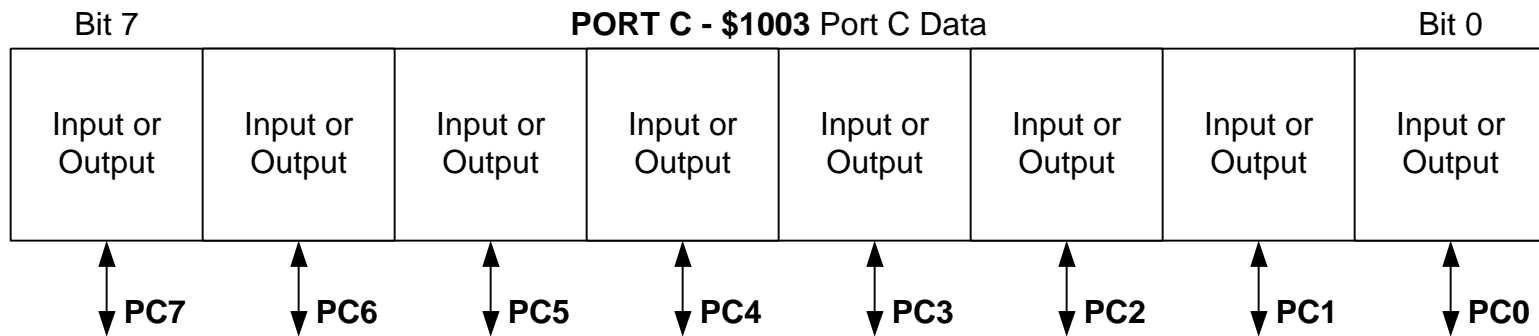
PAEN = Pulse Accumulator System Enable. Disabled = 0, Enabled = 1.

PAMOD, PEDGE, RTR1, and RTR0. Pulse Accumulator and Real Time Clock Control Signals



# Motorola 68HC11 PORT C

- This port can serve as a general-purpose 8-bit bi-directional port with or without handshaking or as a multiplexed address/data bus in expanded mode.
- If an **INPUT** bit is written to, the new value will be recorded in a latch. The new value will be observed at the respective pin, when the pin is reconfigured as **OUTPUT**.

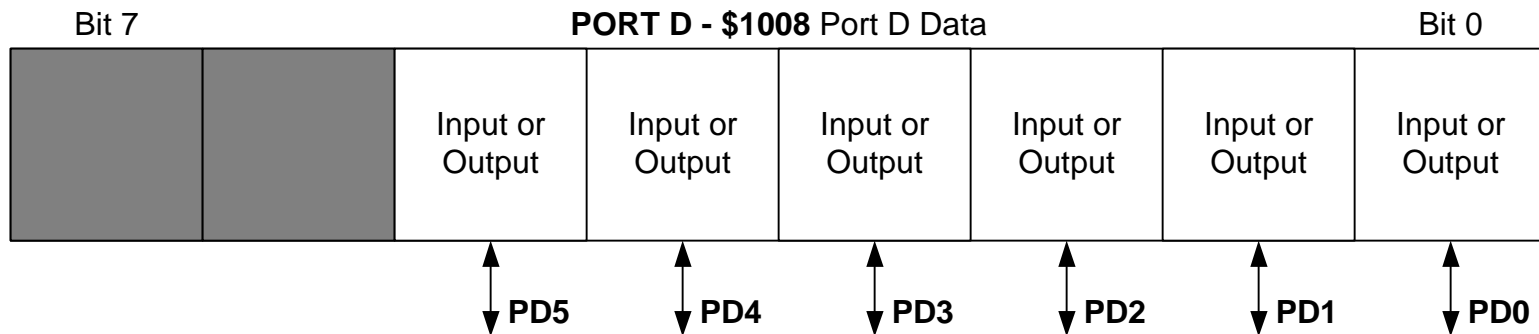


RESET      0      0      0      0      0      0      0      0

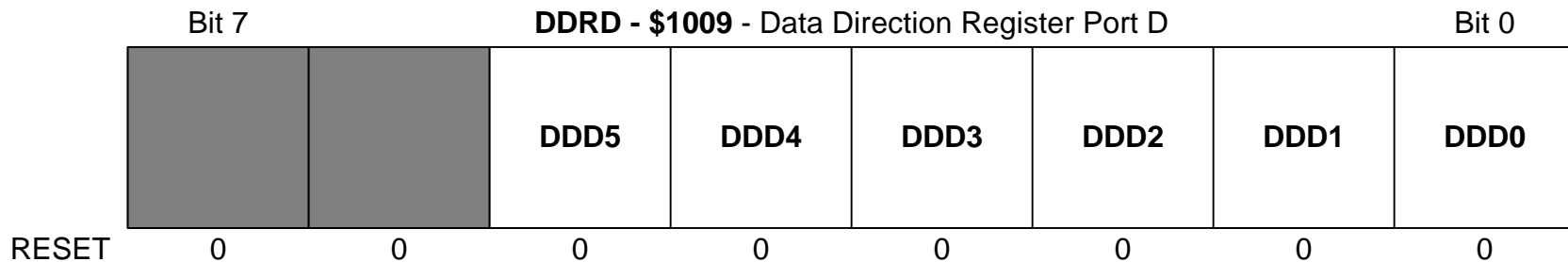
DDCx    Input = 0, Output = 1

# Motorola 68HC11 PORT D

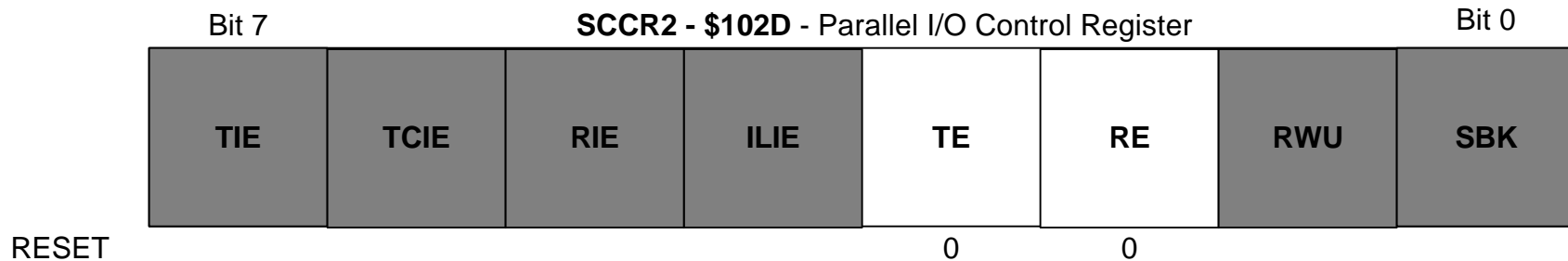
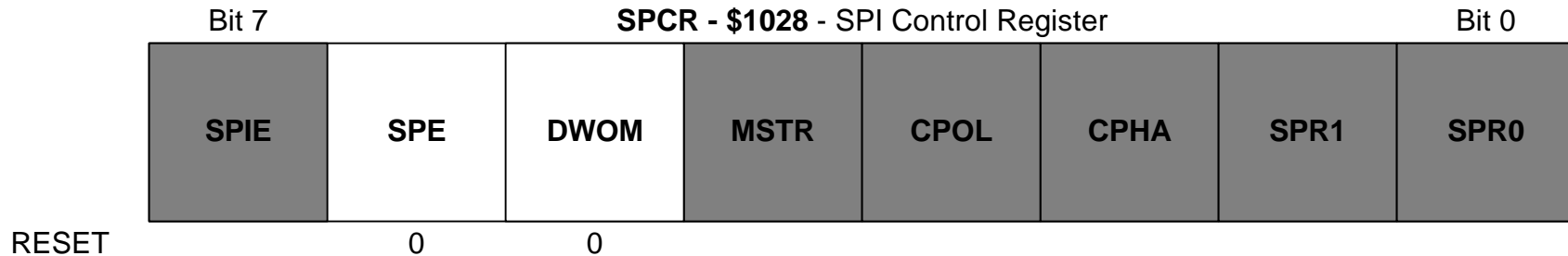
- Port D can serve as six bi-directional bits for digital I/O or it can be associated with serial communications.
- The choice of function for PORT D is done in the SPI Control Register (SPCR) and the SCI Control Register (SCCR2).



DDDx    Input = 0, Output = 1



# Motorola 68HC11 PORT D (Cont.)



**SPE** = SPI System Enable.

0 = Disable

1 = Enable

**DWOM** = Port D Wire-Or Mode.

0 = PORT D outputs normal.

1 = PORT D outputs open drain (pull-up resistors needed).

**TE, RE** = Transmitter and Receiver Enable.

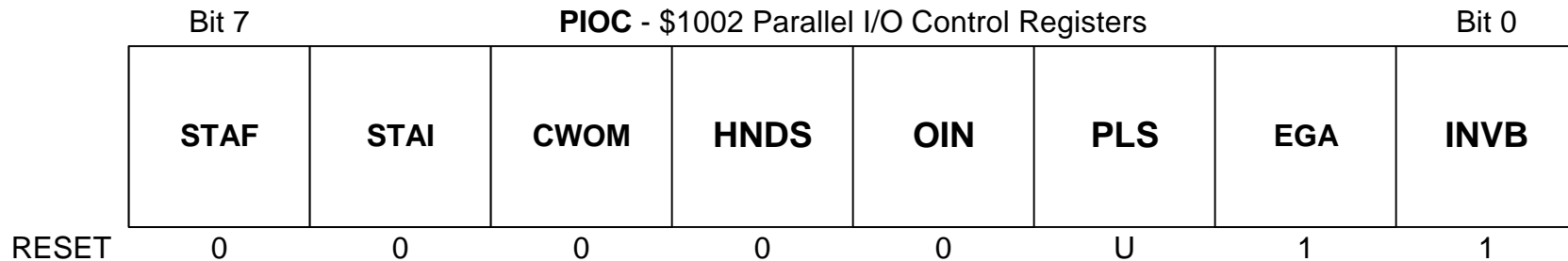
0 = Disable

1 = Enable

WARNING!!!  
EVB Resets this pins with 1 instead of 0!



# Motorola 68HC11: Full Handshake



**HNDS: Handshake Mode.** When *clear*, strobe A acts as a simple input strobe to latch data into PORTCL, and strobe B acts as a simple output strobe which pulses after a write to PORT B. When *set*, a handshake protocol involving PORT C, STRA and STRB is selected (see the definition of the OIN bit).

0 = Simple Strobe mode

1 = Full Input or Output handshaking mode

**OIN: Output or Input Handshaking.** This bit has no meaning when HNDS = 0.

0 = Input Handshake

1 = Output Handshake

**PLS: Pulse/Interlocked Handshake Operation.** This bit has no meaning if HNDS = 0.

0 = Interlocked handshake select. STRB stays activated until STRA.

1 = Pulsed Handshake Select. STRB stays activated for only two E cycles.

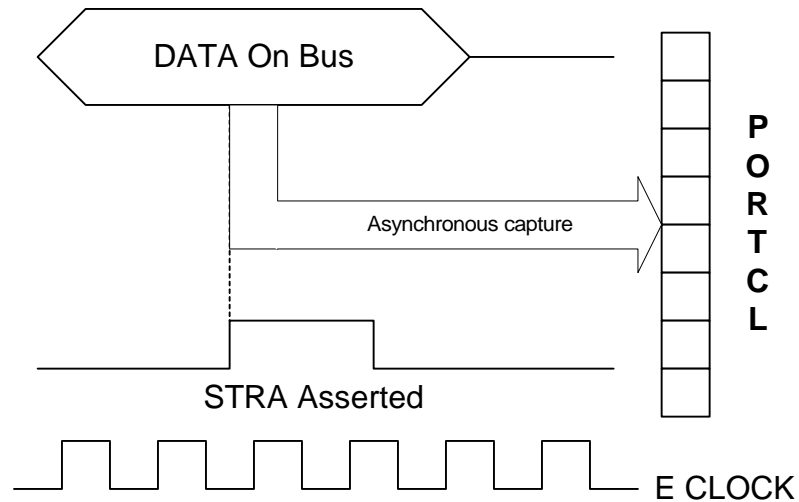
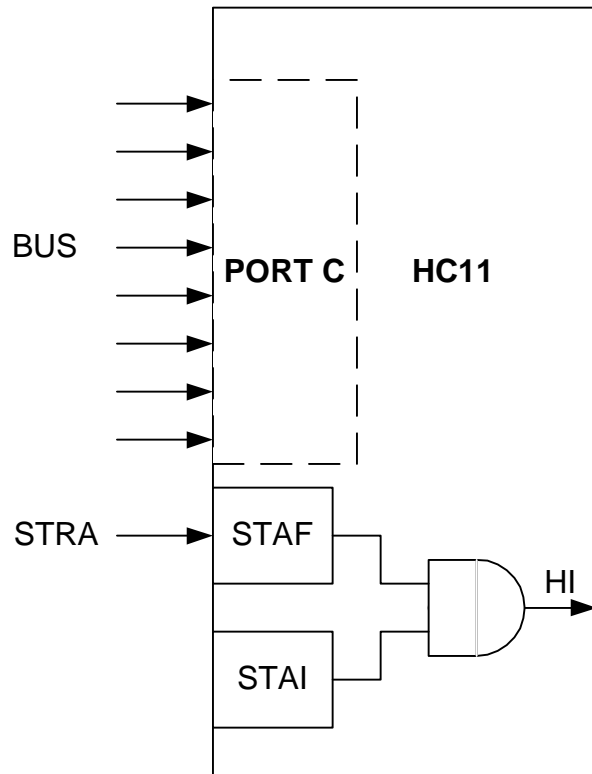
**INVB: Invert Strobe B**

0 = Active level is logic zero

1 = Active level is logic one

# 68HC11 Simple Handshake Examples

HNDS = 0 Simple Input on Port C



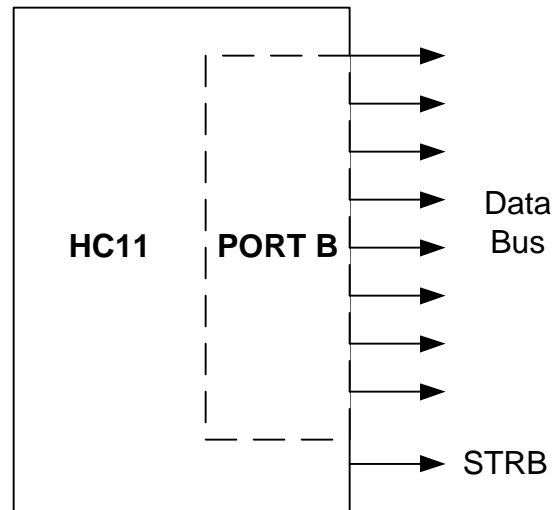
**PORTCL (\$1005)** is loaded with the values entering pins **PC0** to **PC7** as soon as **STRA** is asserted. **STAF** is set with the assertion of **STRA**. If **STAI** is also set, a Hardware Interrupt is issued.

## Simple Strobed Input



# 68HC11 Simple Handshake Examples

HNDS = 0 Simple Output on Port B



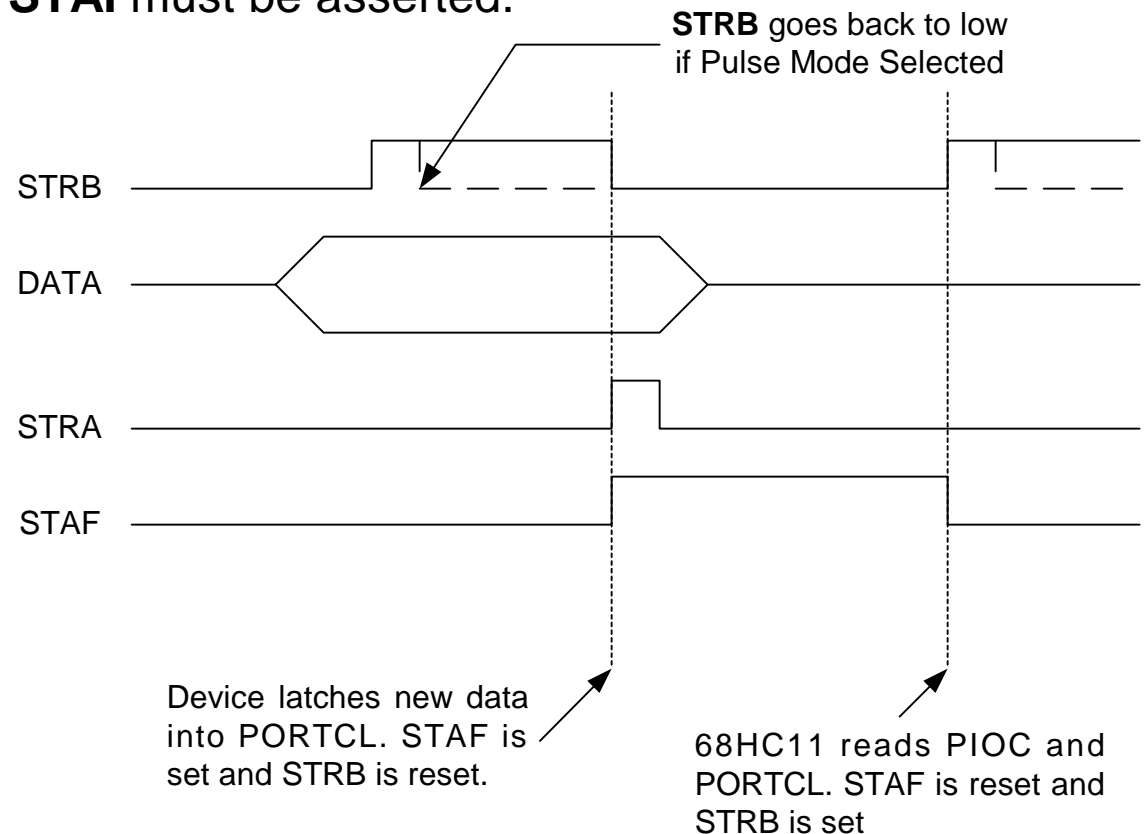
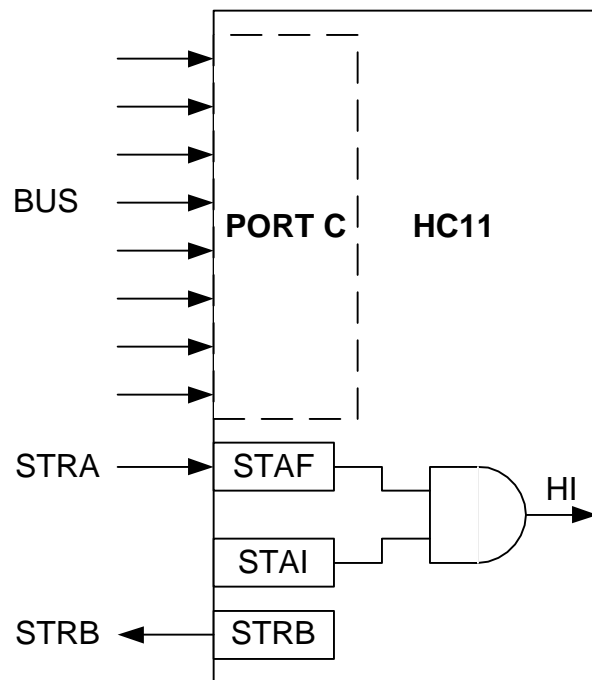
When data is written to **PORT B**, the **STRB** pin is asserted for two E-clock periods. **STRB's** polarity is controlled by the **INV** bit on **PIOC (\$1002)**.

**Simple Strobed Output**

# 68HC11 Full Handshake Example

HNDS = 1, OIN = 0, Full Input Handshaking

- The goal of full Input Handshaking is to prevent the external device from latching new data into **PORTCL** before the CPU has read the old.
- **STRB** (asserted) means that the CPU is ready to read more data. **STRB** is asserted when the CPU reads **PORTCL**.
- **STRA** is asserted by the external device when it latches data into **PORTCL**. **STAF** is asserted and **STRB** is deasserted.
- If a Hardware Interrupt is desired, **STAI** must be asserted.



# 68HC11 Full Handshake Example

## HNDS = 1, OIN = 1 Full Output Handshaking

- The goal of full Input Handshaking is to prevent the 68HC11 from changing data in PORTCL before the external device has taken it.
- **STRB** (asserted) means that data in output is available.
- **STRA** is asserted by the external device when data has been accepted.
- If a Hardware Interrupt is desired, **STAI** must be asserted.
- **STAF** is reset only if **PIOC** is read when **STAI = 1** and then outputting next byte of data to **PORTCL**.

